Amendments to the Specification

Please insert the following header and paragraph on page 1, immediately following the title:

--Cross Reference to Related Applications

This is the U.S. National Stage of International Application No. PCT/JP2004/018054, filed December 3, 2004, which claims the benefit of Japanese Patent Application No. 2003-411068, filed December 9, 2003. These prior applications are incorporated by reference herein.--

Please replace the paragraph beginning at page 1, line 6, with the following rewritten paragraph:

A filter is an indispensable circuit element in signal processing and is the most frequently appearing and most important circuit in digital signal processing. There are two ways to configuring a digital filter, ~~an~~a FIR (Finite Impulse Response) filter and an IIR (Infinite Impulse Response) filter, but the FIR filter which enables a constantly stable characteristic is easier to use (for example, refer to Japanese Patent Application ~~Lied~~Laid-open No.103,418/1984).

Please replace the paragraph beginning at page 1, line 13, with the following rewritten paragraph:

Fig.8 shows an example of a direct form structure, which is one of the most common configurations. In Fig.8, the reference numeral 100 indicates a delay circuit as an input-delay circuit, where the delay circuit 100 merely delays the input data by 1 clock cycle in order to pass it on to the next stage. The reference numeral 101 shows a multiplier as a multiplication circuit, and 102 shows an adder. In this configuration, the data-fetch circuits before and after the delay circuit 100 are each called a "tap", and the number of multipliers 101 connected alongside each other to the data-fetch circuits are called "number of taps", hence Fig.8 is an example of a 7-tap configured FIR filter. The reference numeral 103 indicates an input signal (filter –input data), 104 indicates an input data which is output from the delay circuit 100, then passed on to the

succeeding taps and the other delay circuits 100, 105 indicates an output signal (filter-output data).

Please replace the paragraph beginning at page 5, line 11, with the following rewritten paragraph:

However, the FIR filter of the present invention may be comprised of one initial stage element circuit comprised of one or more of said input delay ~~circuit~~circuits mutually connected in cascade into which filter input data is input, and one or more of said multiplier circuits each of which multiplies one or more input data of the input delay circuit by respective coefficients to make partial output data, and a partial output adder which adds said one or more partial output data mutually to make partial sum data of said one or more multiplier circuits, and one or more intermediate stage element circuits comprised of a plurality of said input delay circuits mutually connected in cascade, into which said initial stage element circuit or the output data from the final stage input delay circuit of said intermediate stage element circuit of the prior stage is input, and one or more of said multiplier circuits which multiply the input data from one or more of said input delay circuits by respective coefficients to make partial output data, and a partial output adder which adds the partial output data from one or more of said multiplier circuits mutually to make partial sum data, and a partial sum delay circuit which delays partial output data of said partial output adder, and a partial sum delay circuit which delays the partial sum data from said partial output adder, and a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data, and a final stage element circuit comprised of one or more of said input delay circuits mutually connected in cascade , into which the output data from the final stage input delay circuit of said intermediate stage element circuit of the prior stage is input, and a plurality of said multiplier circuits which the input data from one or more of said input delay circuits and the output data from the last stage input delay circuit by respective coefficients to make partial output data, and a partial output adder which adds partial output data of said plurality of multiplier circuits mutually to make partial sum data, and a partial sum delay circuit which delays partial sum data of said partial output adder, and a partial sum adder which adds partial sum data delayed by said partial

sum delay circuit and partial sum data of said intermediate stage element circuit of the prior stage to make filter output data, and in this way, in the partial sum delay circuit incorporated in the intermediate stage element circuit and the final stage element circuit, partial sum output data of the element stages from initial stage element circuit to final stage element circuit and inner partial sum data of the element circuit can be synchronized with and added, thus it is possible to realize a tap-slice type FIR filter having an arbitrary order and accuracy (bit number) and capable of high-speed operation of 2 GHz or above, and moreover, owing to the mass-production effect of the element circuits being assembled in 3 parts; the initial stage element circuit, the intermediate stage element circuit, and the final stage element circuit, the cost of the high-end digital filter is easily reducible.

Please replace the paragraph beginning at page 7, line 13, with the following rewritten paragraph:

Meanwhile, an element circuit of the FIR filter of the present invention having one or more of said input delay ~~circuit~~circuits mutually connected in cascade, and one or more of said multiplier circuits which multiply the input data from one or more of said input delay circuits by respective coefficients to make partial output data, and a partial output adder which adds the partial output data from one or more of said multiplier circuits mutually to make partial sum data, may be used for the initial stage element circuits of said FIR filter of the present invention, and in addition an element circuit of the FIR filter of the present invention having a partial sum delay circuit which delays partial output data of said partial output adder, and a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data, may be used for the intermediate stage element circuits of said FIR filter of the present invention, and in addition to the first element circuit, an element circuit of said FIR filter of the present invention having a partial sum delay circuit which delays partial sum data from said partial output adder, and a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and the partial sum data from said intermediate stage element circuit of the prior stage to make filter output data may be used for the final stage element circuit of said FIR filter of the present invention.

Please replace the paragraph beginning at page 9, line 11, with the following rewritten paragraph:

Detailed Description

Please replace the paragraph beginning at page 9, line 32, with the following rewritten paragraph:

According to the present invention, ~~ana~~ FIR filter is configured by 4 sorts of element circuits including the post-processing circuit 4. The input signal (filter input data) is generally input as a multiple-bit digital signal, but in this embodiment, the input signal is divided into two bit groups of the upper and lower, and bit-slice configuration is employed so as to enable bit-slice processing on both groups separately. For example, if the input signal is 24 bits wide, the upper 12 bits are assigned to the upper bit group 5, and the lower 12 bits are assigned to the lower bit group 6. The FIR filter of the present invention is configured by 3 sorts of element circuits 1 to 3 with the exclusion of the post-processing circuit 4, and the reason these 3 sorts of circuits are necessary is because the input and output data of each of the element circuits differ slightly. As illustrated, the 3 sorts of element circuits 1 to 3 are connected in cascade and arranged in sets, and the number of the sets is equal to the number of bit-slices; in this embodiment 2 sets, in the diagram disposed one above the other, to obtain the final output data 10 by processing each of the output signals 11 and 12 from these two element circuit sets with the post- processing circuit 4 as a filter output adder. In addition, the inner multiplier coefficient and the delay degree of the partial sum delay circuit of the element circuits 1 to 3 is designed to be variable, and are made externally settable by the setting signal 9. Meanwhile, the multiplier coefficient of the multiplier in the corresponding tap position of the multipliers of the 2 above mentioned element circuit sets which respectively processes the 2 bit groups must be made aligned (equal) to each other.

Please insert the attached Abstract as the last page of the specification.